JUN 0 3 2002

E UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

K. Gotoh et al.

Art Unit: Not Assigned

Application No.: 10/082,055

Examiner: Not Assigned

Filed: February 26, 2002

Atty. Docket No.: 100021-00074

TEST CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT EFFECTIVELY For:

CARRYING OUT VERIFICATION OF CONNECTION OF NODES

REQUEST FOR APPROVAL OF DRAWING CORRECTION

Commissioner for Patents Washington, D.C. 20231

June 3, 2002

Dear Sir:

Applicants respectfully submit a Request for Approval of Drawing Corrections with the proposed corrections to Figure 6, highlighted in red.

Should any fees be due with respect to this paper, please charge counsel's Deposit Account No. 01-2300.

> Respectfully submitted, ARENT FOX KINTNER PLOTKIN & KAHN, PLLC

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BKS/bgk

Enclosures: Corrected Figure 6